



**Agilent Technologies**

**Advanced Design System 2002**  
**WLAN DesignGuide**

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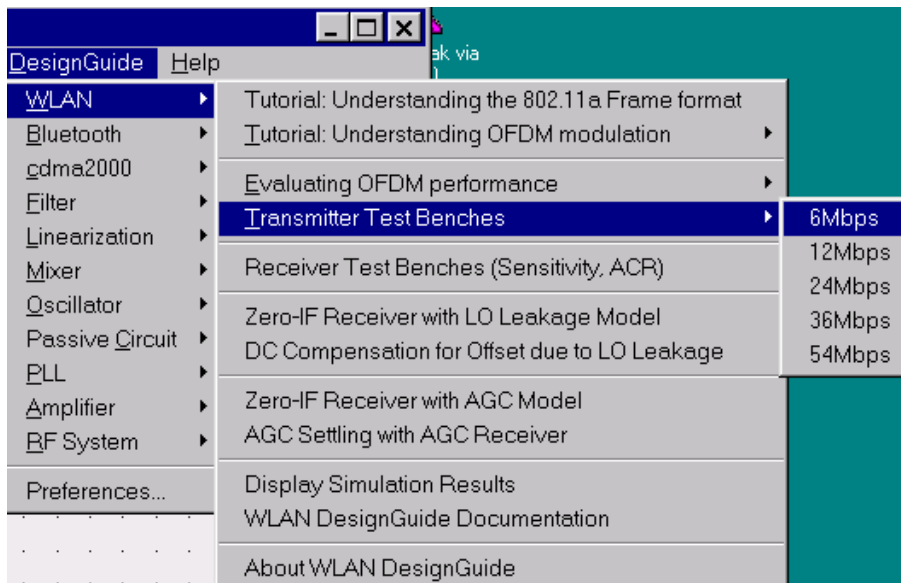
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# Chapter 1: WLAN DesignGuide Basics

The WLAN DesignGuide, accessed from the Advanced Design System Schematic window, provides a convenient set of applications for use with the WLAN Design Library, which is compliant with the 802.11a specification. Examples are also provided with the WLAN Design Library by selecting *File > Example Project > WLAN* from the ADS Main window.



This chapter provides a brief section about some setup features common to all DesignGuides, followed by an overview of the WLAN Design Guide contents.

For detailed reference information, refer to [Chapter 2, WLAN DesignGuide Reference](#).

## Using DesignGuides

All DesignGuides can be accessed in the Schematic window through either cascading menus or dialog boxes. You can configure your preferred method in the Advanced Design System Main window. Select the *DesignGuide* menu.

The commands in this menu are as follows:

**DesignGuide Studio Documentation > Developer Studio Documentation** is only available on this menu if you have installed the DesignGuide Developer Studio. It brings up the DesignGuide Developer Studio documentation. Another way to access the Developer Studio documentation is by selecting *Help > Topics and Index > DesignGuides > DesignGuide Developer Studio* (from any ADS program window).

**DesignGuide Developer Studio > Start DesignGuide Studio** is only available on this menu if you have installed the DesignGuide Developer Studio. It launches the initial Developer Studio dialog box.

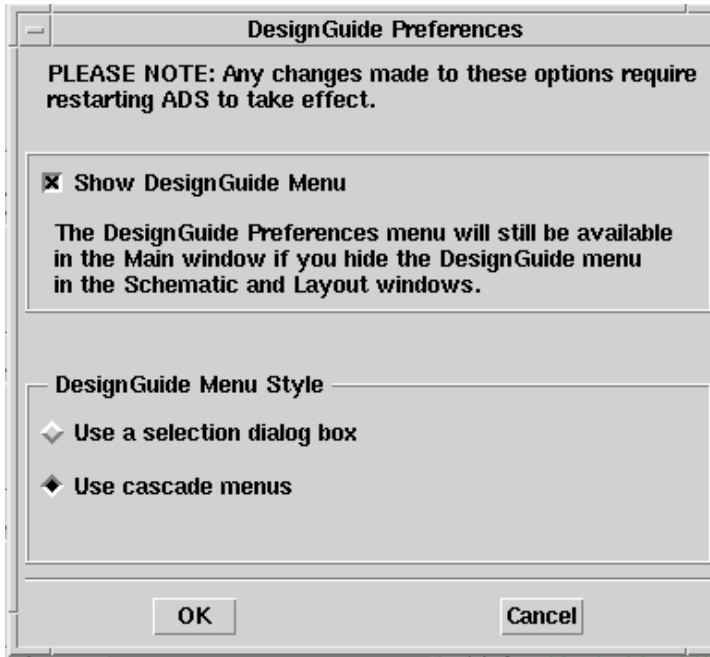
**Add DesignGuide** brings up a directory browser in which you can add a DesignGuide to your installation. This is primarily intended for use with DesignGuides that are custom-built through the Developer Studio.

**List/Remove DesignGuide** brings up a list of your installed DesignGuides. Select any that you would like to uninstall and choose the *Remove* button.

## Setting Preferences

**Preferences** brings up a dialog box that allows you to:

- Disable the DesignGuide menu commands (all except Preferences) in the Main window by unchecking this box. In the Schematic and Layout windows, the complete DesignGuide menu and all of its commands will be removed if this box is unchecked.
- Select your preferred interface method (cascading menus vs. dialog boxes).



Close and restart the program for your preference changes to take effect.

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**Note** On PC systems, Windows resource issues might limit the use of cascading menus. When multiple windows are open, your system could become destabilized. Thus the dialog box menu style might be best for these situations.

---

## Accessing the Documentation

To access the documentation for the DesignGuide, select either of the following:

- **DesignGuide > WLAN > WLAN DesignGuide Documentation** (from ADS Schematic window)
- **Help > Topics and Index > DesignGuides > WLAN** (from any ADS program window)

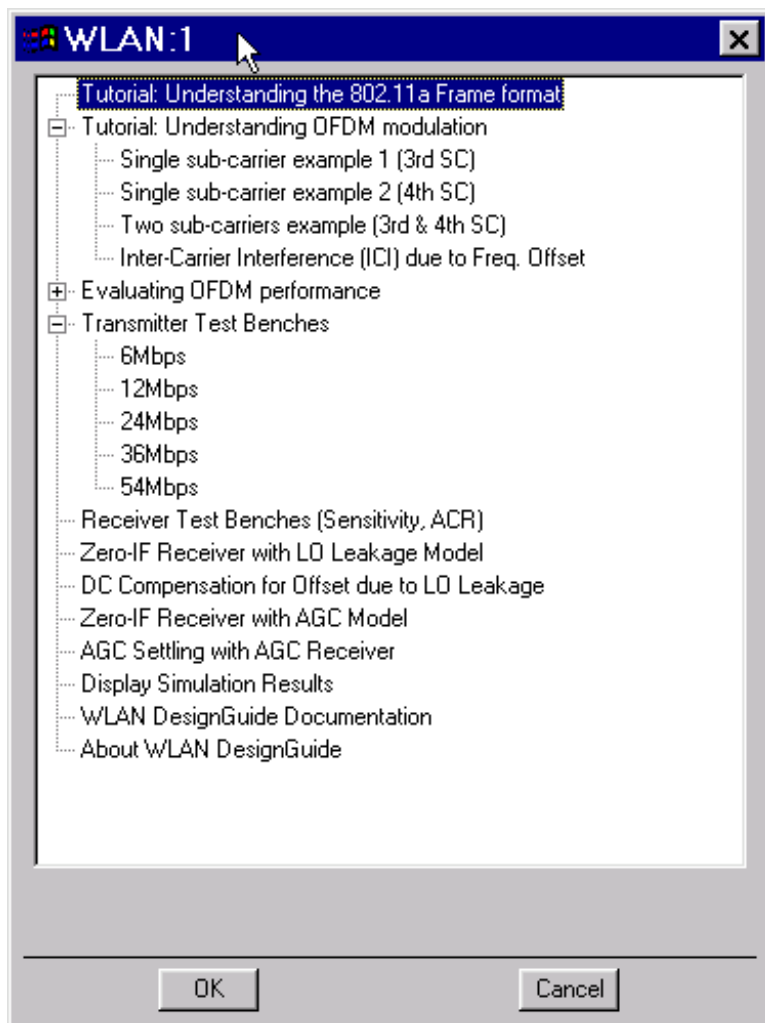
# Summary of WLAN DesignGuide Features

Following are the features of the WLAN DesignGuide.

- *Tutorials Concerning the OFDM and the 802.11a Standard*
  - OFDM Modulation using IFFT and FFT
  - Inter-carrier Interference
  - 802.11a Frame Structure
- *Transmitter Test Benches*
  - Pre-configured sources at various data rates
- *Test Templates to allow evaluation of OFDM modulation under various link impairments*
  - Frequency offset between transmitter and receiver
  - Oscillator phase noise
  - Fixed point effect in FFT/IFFT implementation
  - Power amplifier non-linearity
  - Multipath propagation
  - Transmit Spectrum
  - EVM
  - Receiver Sensitivity
  - Receiver Adjacent Channel Rejection
  - Receiver Alternate Channel Rejection
  - Receiver Maximum Input Power
- *Zero-IF Receiver and associated Test Benches*
  - The Zero-IF receiver topology in 802.11a systems enhances economy, complexity and performance. But it tends to generate DC offsets due to Local Oscillator (LO) leakage. Also, an Automatic Gain Control (AGC) capability is required in any receiver implementation. The WLAN DesignGuide provides two test benches that can be used to investigate these effects: LO-leakage / DC-offset compensation and AGC.



The following WLAN DesignGuide menu is shown as it appears when you have configured your program for dialog box access vs. cascading menus, as described in the section “[Setting Preferences](#)” on page 1-2.



For more details on these features, refer to [Chapter 2, WLAN DesignGuide Reference](#).



# Chapter 2: WLAN DesignGuide Reference

This chapter provides reference information on the features included in the WLAN DesignGuide. For an overview of the primary menu and dialog box options, refer to [Chapter 1, WLAN DesignGuide Basics](#).

## The 802.11a Standard

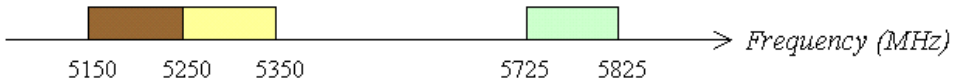
This section provides an overview of the 802.11a Standard, which the WLAN DesignGuide complies with.

### History of the 802.11a Standard

- 802.11 was adopted in July 1997 as a worldwide standard.
  - Supports 1 & 2 Mbps operation at 2.4 GHz band
  - Physical layers: DSSS, FHSS & Infrared
- 802.11b high rate extension adopted in 1999
  - Supports 5.5Mbps and 11Mbps at 2.4GHz
  - CCK modulation, bandwidth compatible with DSSS
- 802.11a specs approved at the beginning of year 2000
  - Supports up to 54Mbps at 5GHz band
  - Uses OFDM modulation

## Frequency Allocations

Following is a summary of the frequency allocations for this standard.



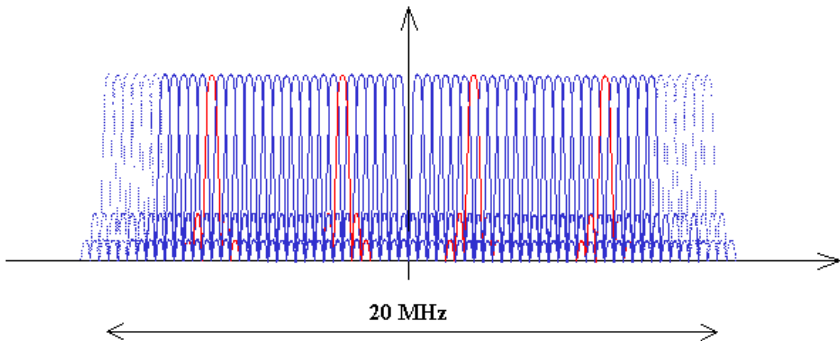
**Unlicensed frequency bands for WLAN in 5GHz. Benign interference situation to be expected compared with the ISM bands in 2.4 GHz.**

**Spectrum globally available.**

**Lower band- 5150-5250 Europe, North America, Japan**

**Middle band- 5250-5350 Europe, North America**

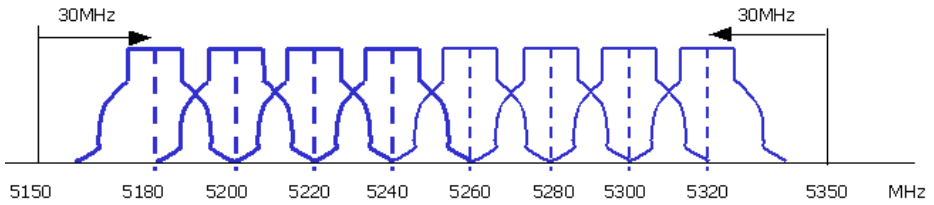
**Upper band- 5725-5825 North America, 5470-5725 Europe**



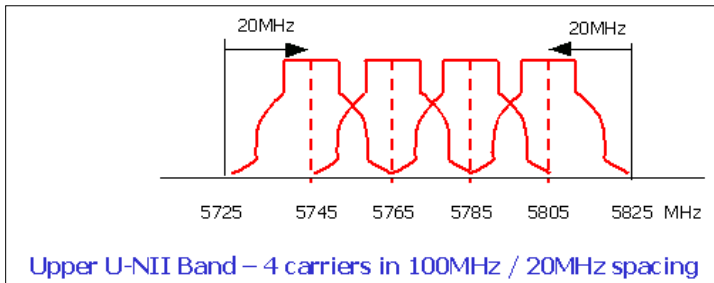
- Modulation: OFDM
- Uses 52 subcarriers: 48 data + 4 pilots
- Convolutional coding rate: 2/3
- The carriers can be BPSK, QPSK, 16QAM or 64QAM modulated. The RF bandwidth is approximately 16.6Mhz.
- OFDM frame duration: 4 $\mu$ s with guard interval: 0.8 $\mu$ s
- Data rate: 6, 9, 12, 18, 24, 36, 48, 54Mbps (6, 12 and 24Mbps mandatory)

# OFDM Signal Spectrum

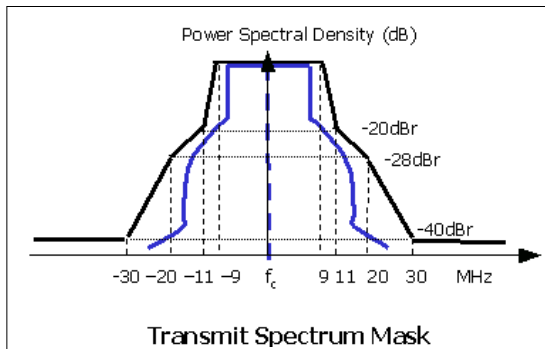
Following are examples of OFDM Signal Spectrum.



Lower and Middle U-NII Band – 8 carriers in 200MHz / 20MHz spacing

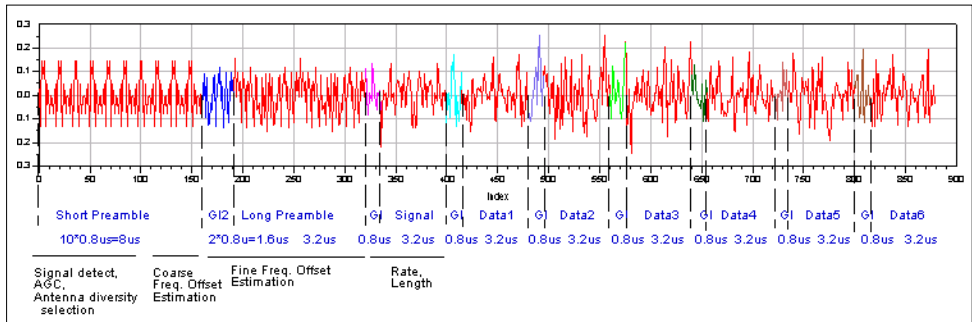
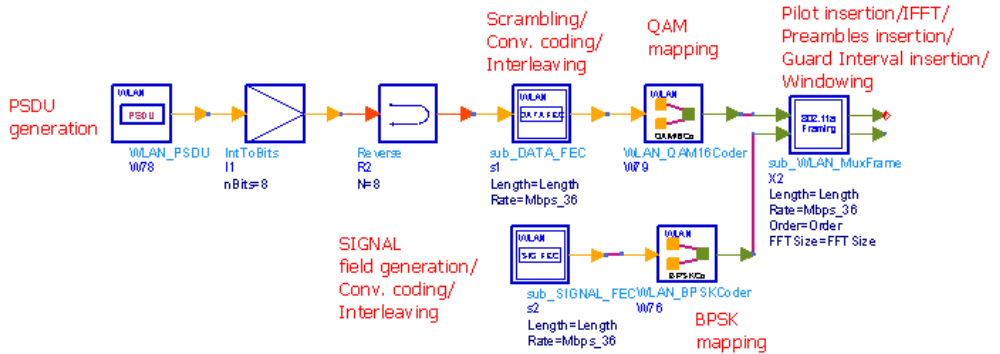


Upper U-NII Band – 4 carriers in 100MHz / 20MHz spacing



# Generating an 802.11a Frame Using ADS

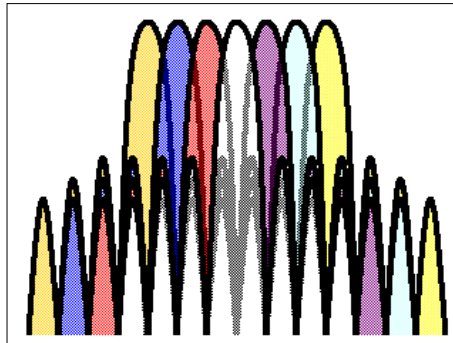
Select Tutorial: Understanding the 802.11a Frame Format.



# OFDM Modulation

Following is a summary of OFDM Modulation.

## Concepts of OFDM



- A type of multi-carrier modulation
- Single high-rate bit stream is converted to low-rate  $N$  parallel bit streams
- Each parallel bit stream is modulated on one of  $N$  sub-carriers
- Each sub-carrier can be modulated differently, e.g. BPSK, QPSK or QAM
- To achieve high bandwidth efficiency, the spectrum of the sub-carriers are closely spaced and overlapped
- Nulls in each sub-carrier's spectrum land at the center of all other sub-carriers (orthogonal)
- OFDM symbols are generated using IFFT

## Advantages of OFDM

- Robustness in multipath propagation environment
- More tolerant to delay spread:
- Due to the use of many sub-carriers, the symbol duration on the sub-carriers is increased, relative to delay spread.

- Intersymbol interference is avoided through the use of guard interval.
- Simplified or eliminate equalization needs, as compared to single carrier modulation.
- More resistant to fading. FEC is used to correct for sub-carriers suffer from deep fade.

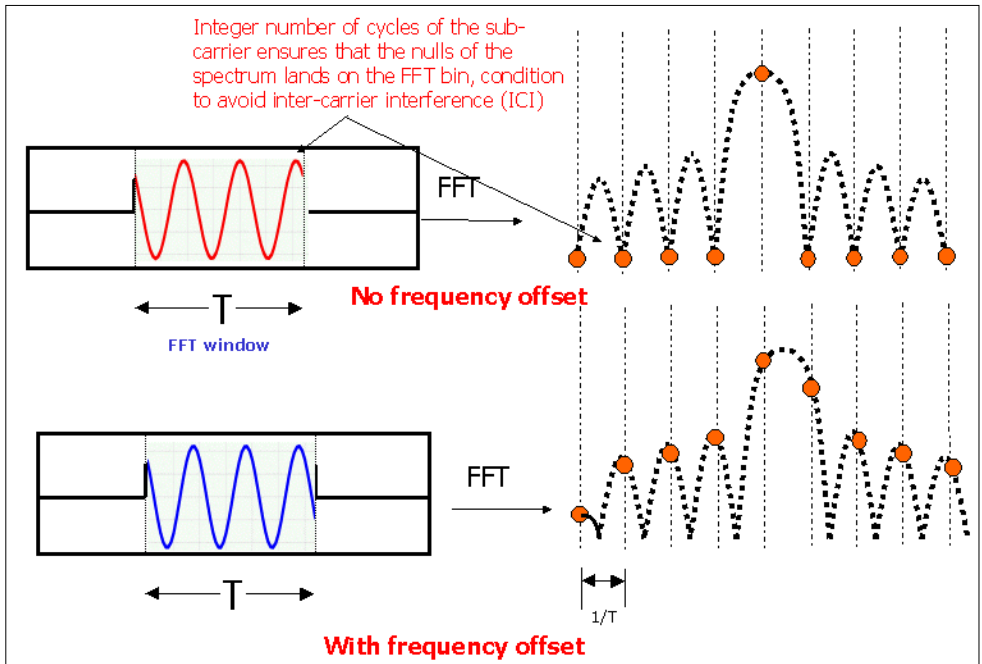
## **Design Challenges of OFDM modulation**

- Sensitive to frequency offset; need frequency offset correction in the receiver.
- Sensitive to oscillator phase noise- clean and stable oscillator required.
- Large peak to average ratio; amplifier back-off, reduced power efficiency.
- IFFT/FFT complexity; fixed point implementation to optimize latency and performance.
- Intersymbol Interference (ISI) due to multipath; use guard interval.

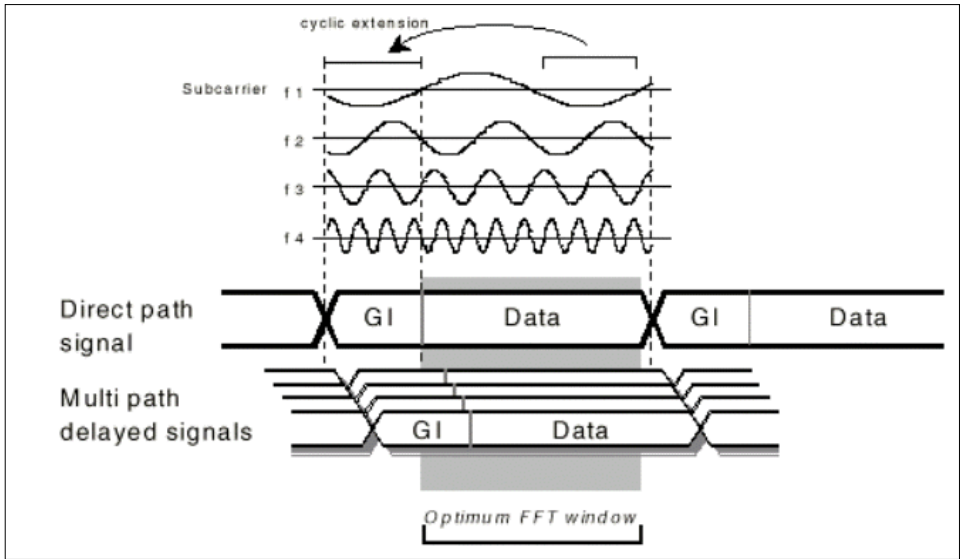


# Inter-Carrier Interference(ICI) Due to Frequency Offset

Select Tutorial: Understanding OFDM Modulation > Inter-Carrier Interference (ICI) due to Freq. Offset.

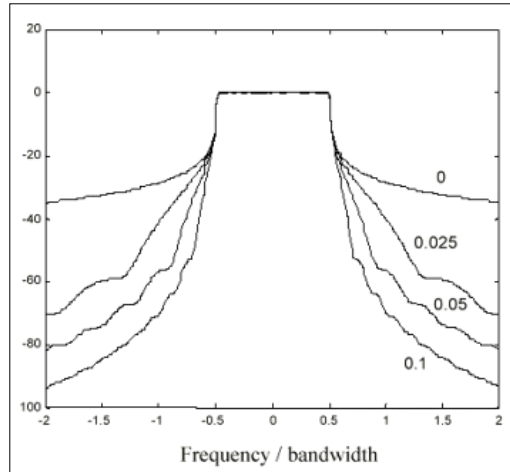


## Guard Interval (GI)



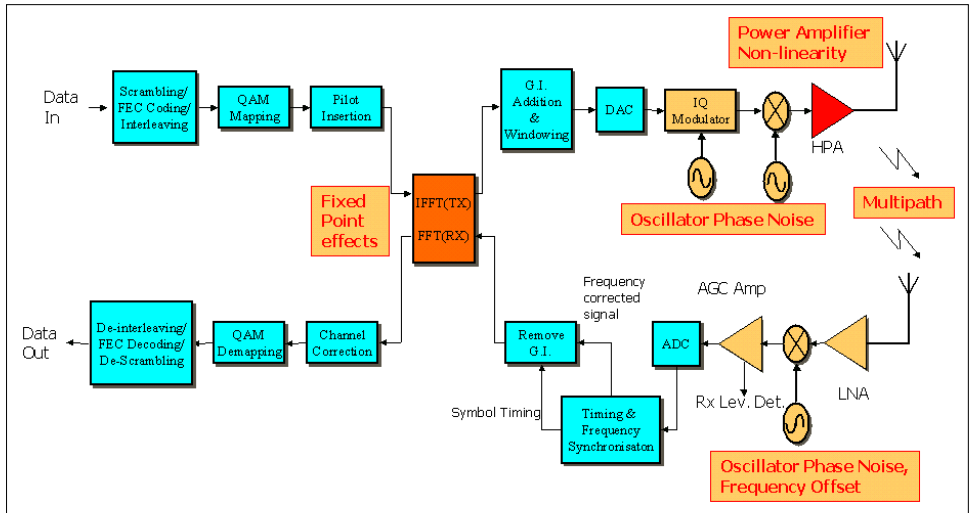
- Multipath delays up to the guard time do not cause Inter-Symbol Interference.
- Subcarriers remain orthogonal for multipath delays up to guard time (no Inter-Carrier Interference).

## Windowing



- To reduce spectrum splatter, the OFDM symbol is multiplied by a raised-cosine window,  $w(t)$  before transmission to more quickly reduce the power of out-of-band subcarriers.
- Preceding illustration shows spectra for 64 subcarriers with different values of the rolloff factor,  $\beta$  of the raised cosine window.
- Larger  $\beta$ , better spectral roll-off.
- However, a roll-off factor of  $\beta$  reduces delay spread tolerance by a factor of  $\beta T_S$ .

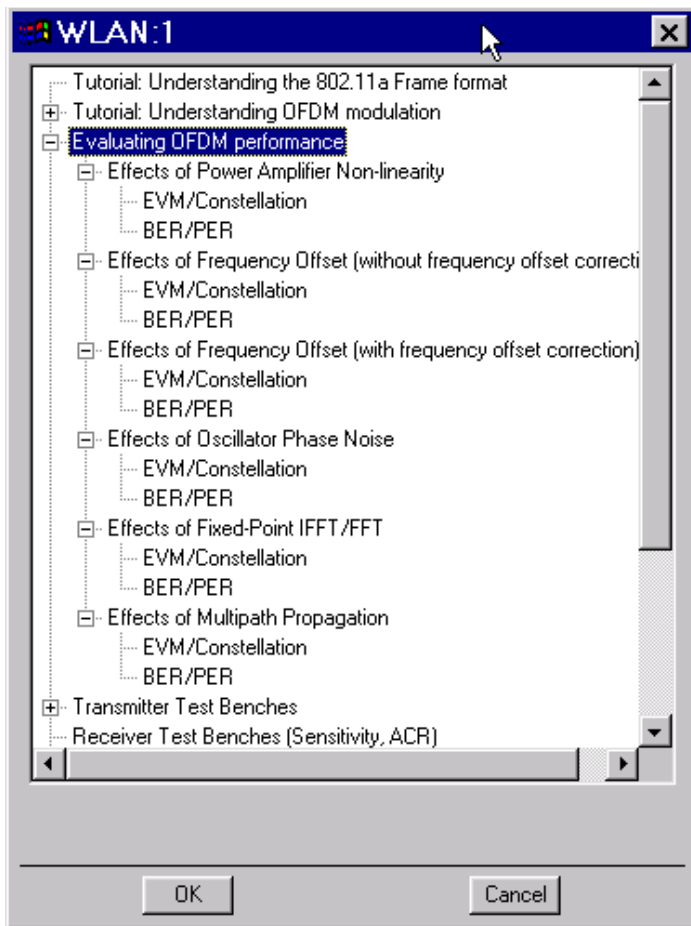
## OFDM Transceiver Block Diagram



## Effects of Link Impairments on OFDM Modulation

This section summarizes the evaluation of the effects of link impairment when using the WLAN Design Library and the WLAN DesignGuide.

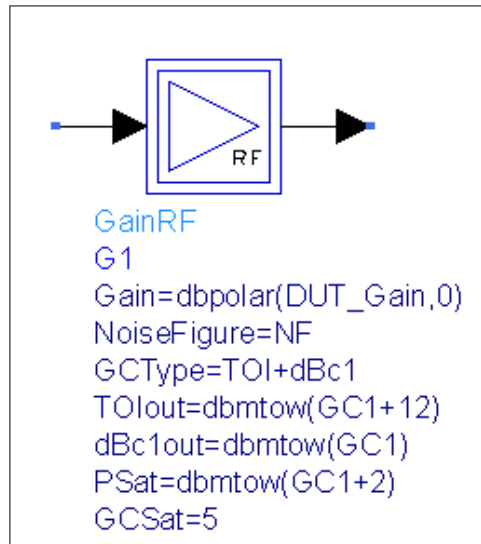
The following WLAN DesignGuide menu is shown as it appears when you have configured your program for dialog box access vs. cascading menus as described in the section [“Setting Preferences” on page 1-2](#).



## Effects of Power Amplifier Nonlinearity

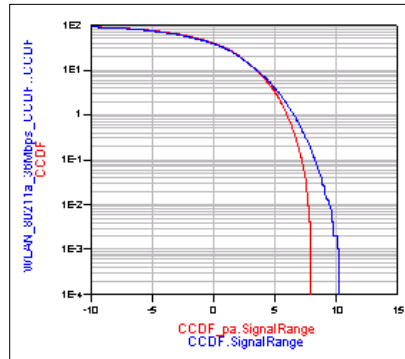
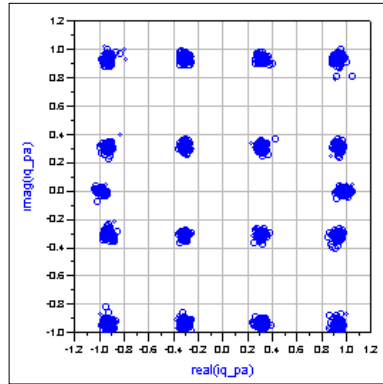
Select **Evaluating OFDM Performance > Effect of Power Amplifier Non-Linearity > EVM/Constellation**.

Following is the Behavioral model used in the PA non-linearity simulation:



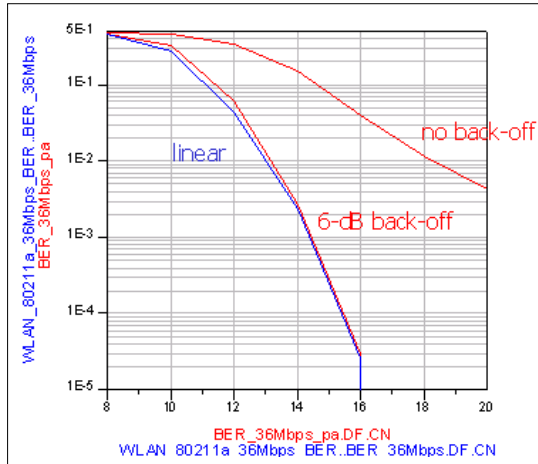
Here the output 1-dB Compression Point (dBc1out) is used along with the output Third-Order Intercept (TOIout) derived from it by adding 12 dB. The results can be evaluated for their effect on EVM (Error Vector Magnitude), Constellation diagram, spectrum and CCDF (Complementary Cumulative Density Function).

Here is a Constellation diagram at 6 dB backoff:



CCDF indicates the probability (starting from 100%) of the signal's peak value in dB. The CCDF plot for the Power Amplifier response, operated at 6 dB backoff from saturation, indicates signal clipping at 7.8 dB, compared to the unamplified signal's peak of 9.4 dB at 0.01%.

The (BER) Bit Error Rate and Packet Error Rate (PER) can also be measured against a particular impairment. For the non-linear PA, the BER can be shown to degrade when the amplifier is not sufficiently backed-off, as shown here.



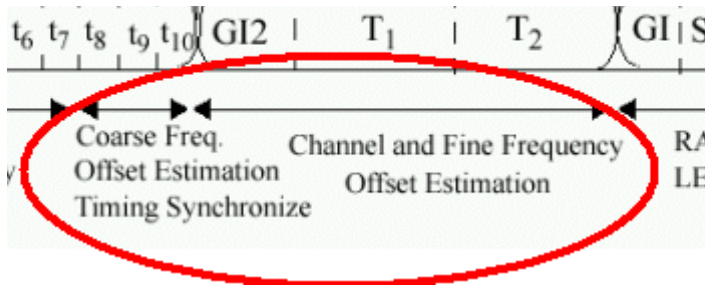
## Requirement for BER/PER Simulations

Due to the use of coding and the presence of non-linear impairments, a Monte Carlo BER simulation method must be used. Since a PSDU length of 1,000 bits is required, these simulation can be quite lengthy. Therefore, most of the saved datasets included with this DesignGuide reflect simulations performed with a much smaller length, e.g. 10 or 100, and will show degradation as the signal is more greatly impaired in some way. However, reliable estimates of the BER or PER for less-impaired signal will require multiple 1,000-bit packets to be simulated.

## Effects of Frequency Offset

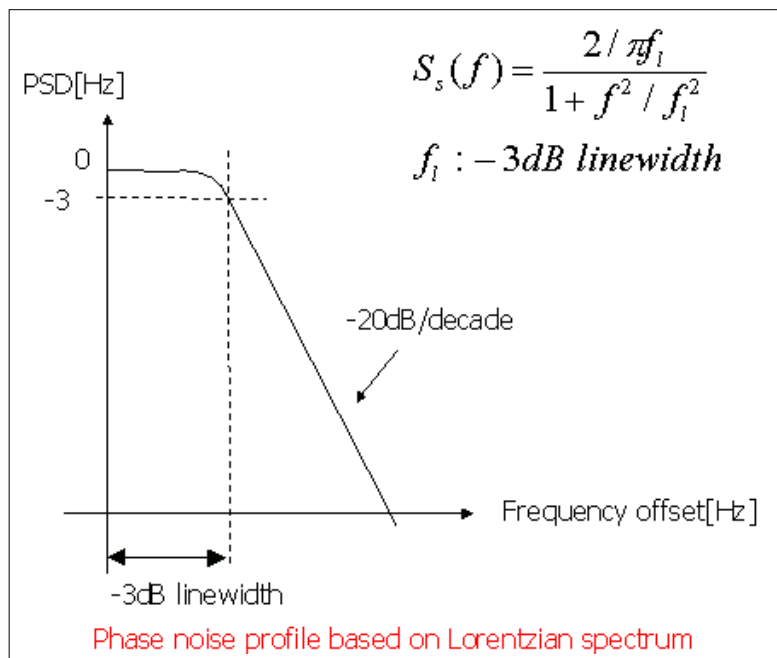
Frequency offset due to differences between the transmit and receive reference oscillators is expressed as a percentage of the 312.5 kHz sub-carrier frequency spacing. The Receiver can perform frequency offset estimation and correction using preambles:



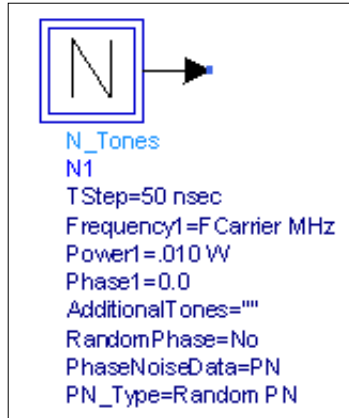


- Make use of short preamble for coarse frequency offset estimation and long preamble for fine frequency offset estimation.
- Short preamble symbol duration of  $0.8\mu\text{s}$  allows frequency correction up to  $1/(2 \times 0.8\mu\text{s}) = \pm 625\text{kHz}$
- Assume RF frequency =  $5.8\text{GHz}$ , the tolerable frequency offset (worst case)  $= 0.5 \times 625\text{k} / 5.8\text{G} = \pm 53.8\text{ppm} > \pm 20\text{ppm}$  specified in 802.11a.

## Effects of Oscillator Phase Noise



An N\_Tones model is used to model the phase noise.

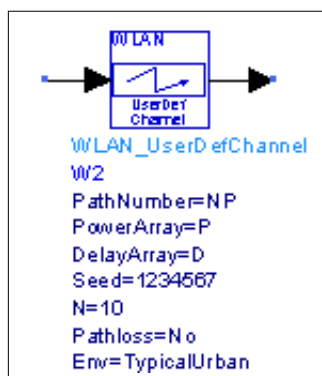


## Effects of Fixed Point implementation of IFFT/FFT

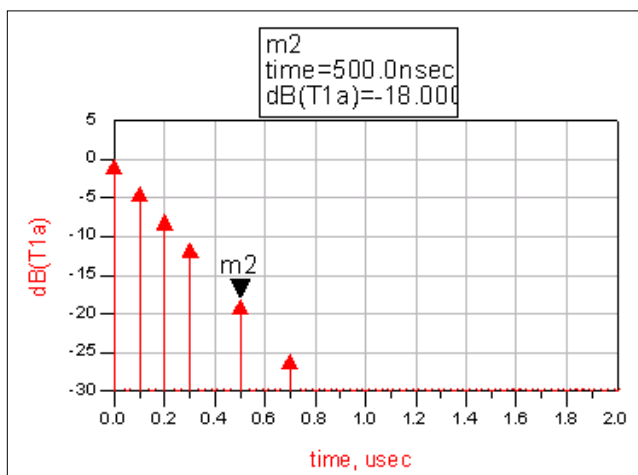
The IFFT and FFT function in the transceiver will have a fixed bit-width. This might have an effect on the system performance. The WLAN DesignGuide provides a 64-point implementation which uses the bit width as a parameter, so it can be changed or swept. It uses a decimation in frequency, Radix-2 algorithm.

## Effects of Multipath

Multipath propagation is simulated using the User-Defined channel model:



This defines an impulse response such as the following.



The RMS Delay Spread, defined as follows, is varied. Typical values are 100-200 nsec.

$$\bar{\tau} = \frac{\sum_k P(\tau_k) \tau_k}{\sum_k P(\tau_k)}$$
$$\tau^2 = \frac{\sum_k P(\tau_k) \tau_k^2}{\sum_k P(\tau_k)}$$
$$\sigma_\tau = \sqrt{\tau^2 - (\bar{\tau})^2}$$

## Receiver Test Benches

### 802.11a Receiver Specifications- Sensitivity

Defined as the minimum RF signal level required to achieve a Packet Error Rate (PER) <10% at PSDU length of 1,000 bytes.

### 802.11a Receiver Specifications-Adjacent Channel Rejection

The desired signal's strength is set at 3dB above the rate-dependent sensitivity, the interfering signal is raised until 10% PER is caused for a PSDU length of 1,000 bytes. The power difference between the interfering signal and the desired signal is the adjacent channel rejection.

---

**Note** Due to the increased bandwidth required by Adjacent and Alternate channel simulations, it is necessary to decrease the simulation time step by a factor of 2 to 4 times, and to increase the order of the IFFT/FFT from 6 to 8 or 9. The simulation time will correspondingly increase with these changes. Also, at this time data displays and datasets might not be provided for some of the Alternate channel test benches.

---

## 802.11a Receiver Specifications-Alternate Channel Rejection

The desired signal's strength is set at 3dB above the rate-dependent sensitivity, the interfering signal is raised until 10% PER is caused for a PSDU length of 1000bytes. The power difference between the interfering signal and the desired signal is the adjacent channel rejection.

## Zero-IF Receiver Test Benches

The Zero-IF receiver topology is desirable for use in 802.11a systems for various reasons of cost, complexity and performance. However, it is prone to generating DC offsets due to Local Oscillator (LO) leakage. Also, an Automatic Gain Control (AGC) capability is required in any receiver implementation. The WLAN DesignGuide provides two test benches that can be used to investigate these effects.

### Receiver LO leakage, DC Offset Compensation Test Bench

Test bench name: *Test\_DCComp\_WLAN\_80211a*

This DesignGuide Receiver uses a direct down-conversion or zero-IF architecture. One problem inherent to the zero-IF architecture is the presence of DC offsets at the mixer output due to LO leakage at the mixer input. The DC offset due to LO leakage is a major factor at low input levels, where the offset can be on the same order of magnitude as the mixer output. This model provides means to evaluate and compensate for LO leakage effects.

In this model, the DC compensation operates on the I and Q outputs of the QAM\_DemodExtOsc block. The DC compensation circuit runs with no input signal present. A switch is located at the receiver input to ensure no signal is present during DC compensation for LO leakage. A delay block has been placed in the signal path between the transmitter and receiver to allow DC compensation to run before the transmitted signal reaches the receiver.

The DC compensation circuit runs for 4 micro-seconds to find the DC level of the I and Q outputs of the QAM\_DemodExtOsc block. Then, the DC levels are latched and subtracted from the respective signals. This method will reduce LO leakage effects assuming that the leakage is constant at the mixer input.

The top-level model includes a transmitter block, a path loss block, a delay block, and a receiver block. Several TimedSink blocks are included to allow detailed evaluation of the receiver and DC compensation performance. The major points of interest included: I\_at\_Mixer\_Output, Q\_at\_Mixer\_Output, I\_Corrected, Q\_Corrected,

I\_ZIF\_Output, and Q\_ZIF\_Output. Two data displays show the outputs of these time sinks. WLAN\_DCComp\_IandQ shows several points along the I and Q chains in the receiver along with the DC compensation for each chain. The plots show the I and Q outputs of the mixer, the detected DC levels, the compensation signals, and the corrected I and Q signals. WLAN\_DCComp\_EVM shows the EVM versus time plot of the receiver output.

Use the parameter sweeps of MixerLOtoRFIsolation and MixerLOtoRFPhaseShift to evaluate the effects of different LO leakage levels and phases. When using these sweeps, it might be necessary to remove some of the traces from the data displays for clarity. No matter what the initial DC offset of I and Q, all the corrected traces lie directly on top of each other and are centered about zero volts. This indicates that the DC compensation will correct any LO leakage level and phase properly.

The receiver used in this model includes an RX Front end (RF filter, T/R Switch, and LNA), a DEM QAM mixer, a DC compensation circuit, and I/Q baseband amplifier/AGC chains. The typical parameters for each stage are defined at the top-level model – LNAGAIN, LNANF, BB2Gain, etc. The receiver uses a perfect AGC, which is modeled using MatchedLoss blocks in the I and Q chains. The loss of these blocks is calculated through the AGCcalc and AGC equations on the top level.

Each DC compensation circuit consists of a splitter, a filter, an inverting amplifier, a sample/hold block, and a combiner. The mixer output is split into two paths; one path goes to the DC compensation combiner and the other goes to the DC detection filter. The filter reduces noise coming from the mixer output in order to determine the DC level of the signal. The output of the filter (detected DC level) is then inverted through the amplifier and input to the sample/hold block. The sample/hold block latches its output 4 micro-seconds after the DC compensation begins. This output is then combined with the original signal, effectively removing the DC component.

It might prove helpful to evaluate the performance of the receiver without DC compensation. To turn DC compensation off, disable all the blocks in the DC compensation model and connect the I and Q outputs of the DEM QAM block to the filters in the I and Q chains respectively.

## Receiver Dynamic Range, CCA and AGC Test Bench

Test bench name: *Test\_AGCSettling\_WLAN\_80211a*

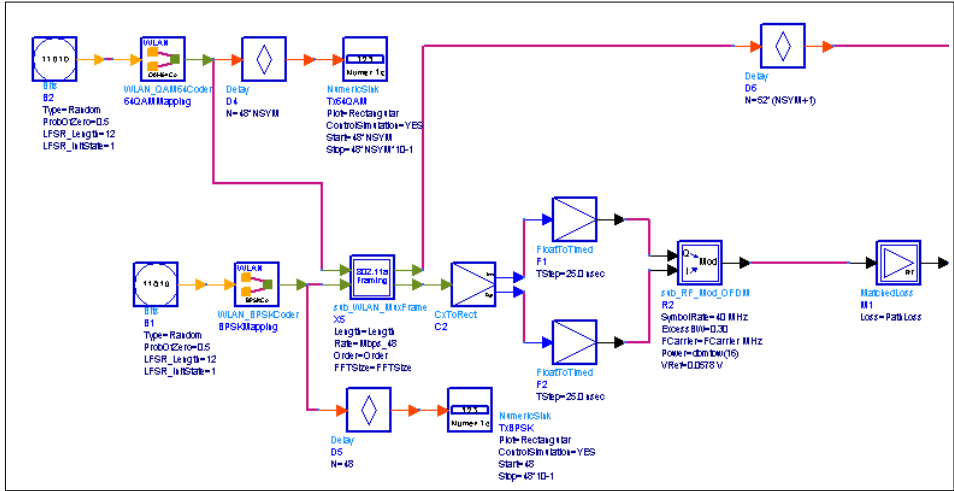
Specification reference: Section 17.3.10.4, Section 17.3.3, Section 17.3.10.5

The 802.11a modulation requires a linear transmitter and receiver chain. This linearity requirement creates a difficult challenge for the receiver design. Typically, an automatic gain control (AGC) is used in the receiver to ensure that the linearity requirements are met. This model includes a fast, digital AGC that settles within ~5  $\mu$ sec. From the 802.11a standard (Section 17.3.3), the receiver design has 8  $\mu$ sec to perform a signal detection, settle AGC, select diversity (if any), run coarse freq offset adjust and timing recovery.

In this model, AGC runs on the first 5-6 short symbols of the preamble, which produce a fairly constant envelope waveform. The variable AGCsettlingtime (in  $\mu$ sec) defines how long AGC runs. Selection of this value is a tradeoff between the dynamic range of the receiver (ie. the dynamic range required of the AGC), AGC step size and step timing, and the aforementioned functions that also need to run in the 8  $\mu$ sec of 10 short symbols.

The top-level model includes a transmitter block, a path loss block, and a receiver block. To run quick simulations to observe various points in the receiver and AGC sections, enable the TKShowValues and TKPlots to observe real-time effects. For a more detailed analyses, disable these blocks and enable the TimedSinks at the various points on the top-level model. The major points of interest include: Filtered\_AGCDetout, RSSI\_CCA\_Indicator, ReceiverEVM, and AGC\_Value. A data display is set up, Test\_AGCSettling\_WLAN\_80211a, which includes the outputs of many of these time sinks. If you are interested in the performance of AGC vs. the entire RX dynamic range, enable the Parameter Sweep for PathLoss and this will sweep the input signal to the receiver from -4 to -64 dBm.





## Following are the variables used in the simulation

:

var  
Eq 1

VAR

VAR5

```

DetOP1dB=0
DCCompDelay=0
Bits=195
Tslice=66.5+DCCompDelay
Ntrainer=50+DCCompDelay
FBDCCompClkPeriod=2.66
FBDCCompClkPeriod2=2.66
InjectedDC=0
MixerLOtoRFPhaseShift=0
MixerLOtoRFIsolation=200
PathLoss=20
Foffset=0
AGCLoss=0

```

var  
Eq 1

VAR

VAR6

```

Data=48
BitsPerSym=1
Tsym=1
SamplePerSym=100
Tstep=2.5/SamplePerSym
TStep=Tstep
AGCsettlingtime=5
Tstart=DCCompDelay
Tstop=Bits+Tstart
RFFiltLoss=2
LNAGain=30
LNANF=2.5
Matchloss=3
BB2Gain=30
BB1Gain=30

```

var  
Eq 1

VAR

VAR2

```

N=int ((16+8*Length+6)/192)
LL=16+8*Length+6-192*N
KK=if (LL==0) then 0 else 1 endif
NSYM=N+KK

```

var  
Eq 1

VAR

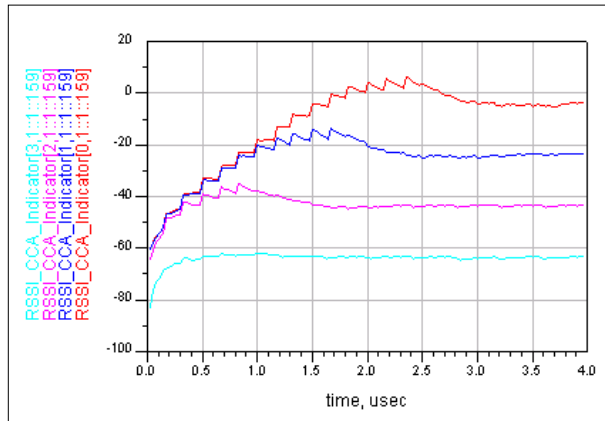
VAR1

```

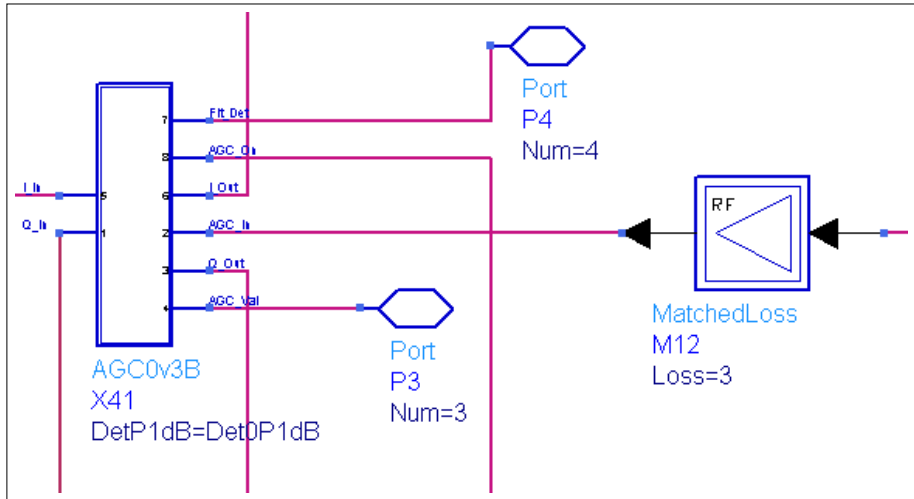
FCarrier=5200
FreqOffset=50
Length=256
Order=7
FFTSize=128

```

The data display shows many key parameters of the 802.11a receiver. One of the most critical items in this design is AGC settling time vs. EVM or BER/PER. The data display shows plots of AGC vs. time, RSSI (Received Signal Strength Indicator) vs. time, EVM vs. time and other important design considerations.



The receiver (push into RECEIVER\_ZIF\_AGC) used in this model includes a RX Front end component (RF filter, T/R Switch, and LNA), a DEM QAM mixer, a pair of linear baseband amplifiers (BB1), followed by an AGC block, with the last blocks being a pair of nonlinear baseband amplifiers (BB2). The typical parameters for each stage are defined at the top-level model: LNAGAIN, LNANF, BB2Gain, etc. For this model it was assumed that the non-linear effects of all stages prior to BB2 could be ignored.



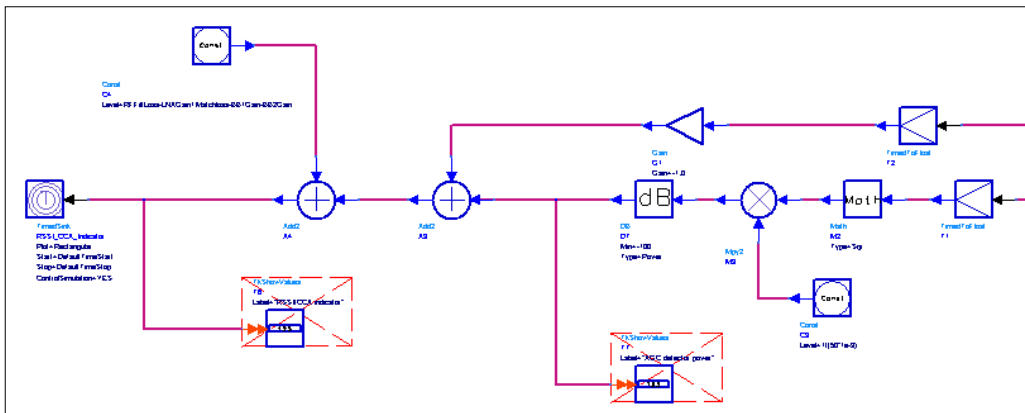
For OFDM systems, like 802.11, there is a large >10 dB, peak-to-average value of the signal. This requires a backoff from P1dB for BB2 to keep this stage from compressing. This backoff is determined by the variable Det0P1dB on the top-level model. This variable defines the output signal level of BB2 that the AGC attempts to maintain. For example, if Det0P1dB=17 dBm, the digital AGC will try to keep the output of BB2 to +17dBm. Consequently, the backoff is determined by BB2 P1dB – Det0P1dB.

As previously mentioned, the digital AGC always tries to keep the output envelope of the BB2 pair at a constant level. It does this by first calculating the signal amplitude, at BB2 output, by the math function  $\text{SQRT}(I^2+Q^2)$ . This level is then compared with five detector levels which control four different AGC states: -5 dB, -1 dB, +1 dB, and +5 dB. The digital AGC works by comparing the input signal amplitude with 5 threshold values and applying an appropriate gain adjustment to attempt to keep BB2's output constant. For example, if the input signal is greater than the defined AGC trip point (ie. Det0P1dB) by >5 dB, then the threshold for the -5 dB AGC is triggered, this results in a 5 dB increase in attenuation for that AGC time step. The next time step, a similar comparison is made. Eventually, if the signal is within the dynamic range of the receiver, AGC should converge between the +1 and -1 dB AGC trip points, when this occurs no more AGC is applied. Similarly, if the signal is too small or AGC overshoots it's defined value, attenuation can be taken out with the +1

and +5 dB stages. Due to its complexity, the AGC is not shown here, but you can push into AGC0v3B to view it after loading the design.

There are a few parameters that the AGC model uses that are important to note. The AGC time step is defined by the clock that feeds the five CounterSyn blocks. AGC can make a step every 167  $\mu$ sec. AGC is disabled or frozen by toggling the Port 8 which disables the AGC step clock. The current AGC model has 96 dB of dynamic range defined by the two constant blocks set to 0 and -96 dB. There are several ports available to monitor, real-time, AGC functions in this model such as detector output.

This model also calculates RSSI/CCA with the blocks in the top-level. These take the measured detector value at the output of BB2, subtract all the linear gains of all the receiver blocks, and add the AGC value to calculate an input referred power.



Specification reference: IEEE802.11a-1999 Sections 17.10.2 and 17.10.3

IEEE802.11a section 17.3.10.2 specifies the requirement for adjacent channel rejection. Section 17.3.10.3 specifies the requirements for alternate channel rejection.

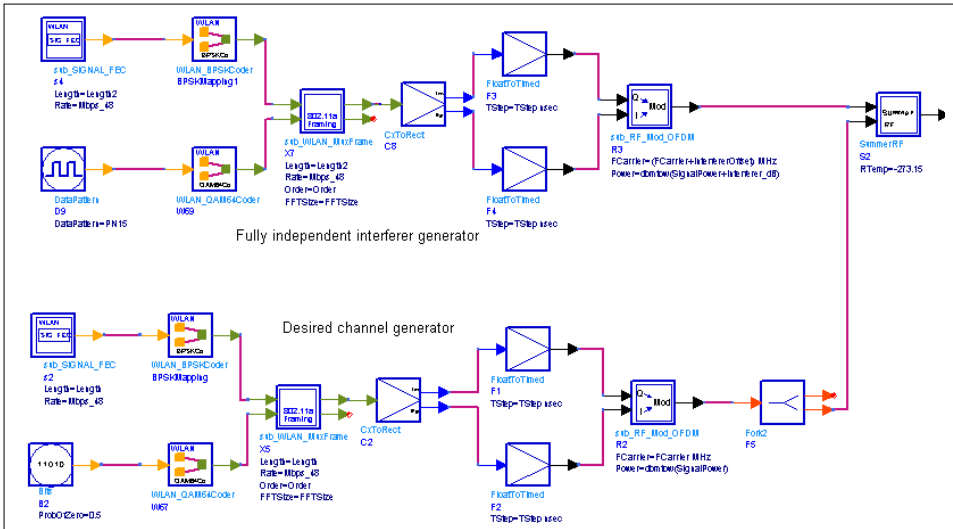
Adjacent channel centers in IEEE 802.11a are off set from the desired channel center by 20 MHz. The alternate channels are offset by 40 MHz.

In this example, the data rate is 48 MHz. To perform adjacent channel rejection testing at this data rate, the specification requires the desired channel power input to the receiver be  $-63$  dBm. An adjacent channel also applied at  $-63$  dBm must not cause the Packet Error Rate (PER) to exceed 10%. To perform alternate channel rejection testing at this data rate, the desired channel power input to the receiver is  $-63$  dBm. An alternate channel applied at  $-47$  dBm must not cause the Packet Error Rate (PER) to exceed 10%.

WLAN library components are used to generate the short preamble, the long preamble, the signal field and the data of the 802.11a transmit signal. The final module in the 802.11a signal generator is the sub\_RF\_Mod\_OFDM block. Transmit filtering is applied at baseband in the sub\_RF\_Mod\_OFDM module and the IQ base band signal is mixed to the RF frequency, specified by the Fcarrier variable. The power level output from the signal generator is set in dBm by the SignalPower variable.

Two options for generating the interferer signal are provided. In one option, the interferer is produced by delaying and amplifying a copy of the desired channel signal. This technique runs more quickly, but results may be affected by correlation between the interferer and desired channels.

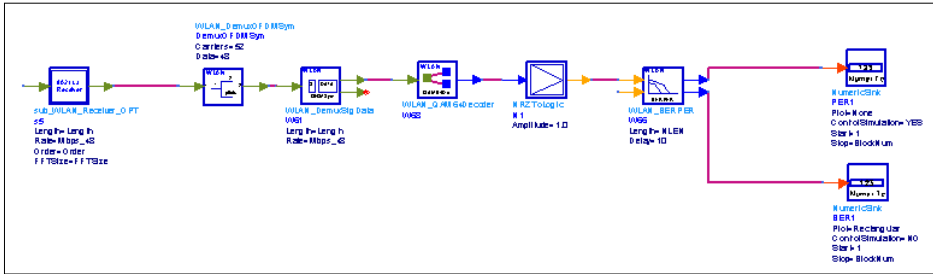
In the second option, a separate 802.11a signal generator is used to produce the interfering signal. To ensure that the desired and interfering channels are uncorrelated, the interferer generator uses a different data set and OFDM packet length than the desired channel. The packet length of the desired signal is set by the Length variable. The packet length of the interferer is set by the "Length2" variable. Using this interferer generation technique, simulations with BlockNum equal to 30 required about 3 times more time to run the same simulations using delayed desired signal as the interferer.



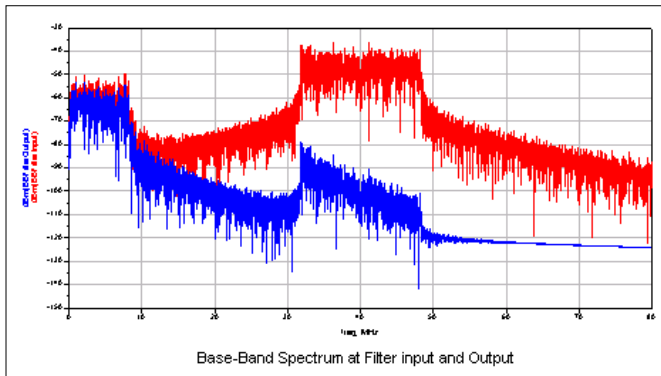
Both options use the *Interferer\_dB* level variable to set the signal level of the interferer in dB relative to the desired signal and the *InterfererOffset* variable to set the frequency offset of the interfering channel from the desired channel in MHz.

The interferer and desired channel signals are combined and input to the Zero IF Receiver block. The RF section of the ZIF receiver represents the loss and gain of filters, matching circuits, and RF amplifiers. Following the receiver RF stage, the desired signal is mixed down to base band IQ signals. Base band filters provide rejection of the interfering adjacent or alternate channel signals. The automatic gain correction of the ZIF receiver is disabled, and fixed gain blocks are installed to replace it. This simplification reduces simulation time and should not affect adjacent or alternate channel rejection. The output of the ZIF receiver goes to amplifier block G6. The signal level required by the demodulation modules of the receiver is a function of the *Order* variable. Gain block G6 provides this required signal level adjustment.

WLAN library components, shown in the figure that follows demodulate the base band IQ signal into digital data. The WLAN\_BERPER module compares the demodulated signal data output to the data input to the signal generator. The Bit-Error-Rate, BER and Packet-Error-Rate, PER, are then calculated. BER and PER are output to data sinks.



The display provides plots of the RF signal spectrum at the input the ZIF receiver input. The spectrum at the filter input and output on one receive base-band signal path is also plotted. A plot also shows the BER and PER values as PPDU frames are received.





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